ESP-ROM:esp32s3-20210327

Build:Mar 27 2021

rst:0x1 (POWERON),boot:0x2a (SPI_FAST_FLASH_BOOT) ESPS3- POWER ON

SPIWP:0xee

mode:DIO, clock div:1

load:0x3fce3818,len:0x1750

load:0x403c9700,len:0x4

load:0x403c9704,len:0xc00

load:0x403cc700,len:0x2e04

entry 0x403c9908

ʦ[0;32mI (27) boot: ESP-IDF 5.1.2 2nd stage bootloaderʦ[0m

ʦ[0;32mI (27) boot: compile time Mar 6 2024 15:28:58ʦ[0m

ʦ[0;32mI (27) boot: Multicore bootloaderʦ[0m

ʦ[0;32mI (30) boot: chip revision: v0.2ʦ[0m

ʦ[0;32mI (34) boot.esp32s3: Boot SPI Speed : 80MHzʦ[0m

ʦ[0;32mI (38) boot.esp32s3: SPI Mode   : DIOʦ[0m

ʦ[0;32mI (43) boot.esp32s3: SPI Flash Size : 8MBʦ[0m

ʦ[0;32mI (48) boot: Enabling RNG early entropy source...ʦ[0m

ʦ[0;32mI (53) boot: Partition Table:ʦ[0m

ʦ[0;32mI (57) boot: ## Label   Usage   Type ST Offset   Lengthʦ[0m

ʦ[0;32mI (64) boot: 0 nvs   WiFi data   01 02 00009000 00006000ʦ[0m

ʦ[0;32mI (72) boot: 1 phy_init   RF data   01 01 0000f000 00001000ʦ[0m

ʦ[0;32mI (79) boot: 2 factory   factory app   00 00 00010000 00100000ʦ[0m

ʦ[0;32mI (87) boot: End of partition tableʦ[0m

ʦ[0;32mI (91) esp_image: segment 0: paddr=00010020 vaddr=3c050020 size=161ach (90540) mapʦ[0m

ʦ[0;32mI (115) esp_image: segment 1: paddr=000261d4 vaddr=3fc96100 size=033ach (13228) loadʦ[0m

ʦ[0;32mI (119) esp_image: segment 2: paddr=00029588 vaddr=40374000 size=06a90h (27280) loadʦ[0m

ʦ[0;32mI (127) esp_image: segment 3: paddr=00030020 vaddr=42000020 size=4fa48h (326216) mapʦ[0m

ʦ[0;32mI (188) esp_image: segment 4: paddr=0007fa70 vaddr=4037aa90 size=0b564h (46436) loadʦ[0m

ʦ[0;32mI (206) boot: Loaded app from partition at offset 0x10000ʦ[0m

ʦ[0;32mI (206) boot: Disabling RNG early entropy source...ʦ[0m

ʦ[0;32mI (218) cpu_start: Multicore appʦ[0m

D (218) flash HPM: HPM with dummy, status is 3ʦ[0m

V (218) mmap: after coalescing, 1 regions are left[0m

[0;32mI (220) octal_psram: vendor id   : 0x0d (AP)[0m

[0;32mI (225) octal_psram: dev id   : 0x02 (generation 3)[0m

[0;32mI (231) octal_psram: density   : 0x03 (64 Mbit)[0m

[0;32mI (236) octal_psram: good-die   : 0x01 (Pass)[0m

[0;32mI (242) octal_psram: Latency   : 0x01 (Fixed)[0m

[0;32mI (247) octal_psram: VCC   : 0x01 (3V)[0m

[0;32mI (252) octal_psram: SRF   : 0x01 (Fast Refresh)[0m

[0;32mI (258) octal_psram: BurstType   : 0x01 (Hybrid Wrap)[0m

[0;32mI (264) octal_psram: BurstLen   : 0x01 (32 Byte)[0m

[0;32mI (269) octal_psram: Readlatency : 0x02 (10 cycles@Fixed)[0m

[0;32mI (275) octal_psram: DriveStrength: 0x00 (1/1)[0m

D (280) MSPI Timing: 0, good[0m

D (283) MSPI Timing: 1, good[0m

D (286) MSPI Timing: 2, bad[0m

D (289) MSPI Timing: 3, good[0m

D (292) MSPI Timing: 4, good[0m

D (295) MSPI Timing: 5, good[0m

D (298) MSPI Timing: 6, good[0m

D (301) MSPI Timing: 7, good[0m

D (304) MSPI Timing: 8, bad[0m

D (307) MSPI Timing: 9, good[0m

D (310) MSPI Timing: 10, good[0m

D (313) MSPI Timing: 11, good[0m

D (316) MSPI Timing: 12, good[0m

D (319) MSPI Timing: 13, good[0m

D (322) MSPI Timing: tuning success, best point is index 5[0m

[0;32mI (327) MSPI Timing: PSRAM timing tuning index: 5[0m

[0;32mI (333) esp_psram: Found 8MB PSRAM device[0m

[0;32mI (337) esp_psram: Speed: 80MHz[0m

V mmu_psram: Instructions from flash page3 copy to SPIRAM page0, Offset: 3

V (382) mmu_psram: after copy instruction, page_id is 5[0m

[0;32mI (382) mmu_psram: Instructions copied and mapped to SPIRAM[0m

V (382) esp_psram: after copy .text, used page is 5, start_page is 5, psram_available_size is 8060928 B[0m

V mmu_psram: Rodata from flash page1 copy to SPIRAM page5, Offset: -4

V (411) mmu_psram: after copy rodata, page_id is 7ᵀ[0m

ᵀ[0;32mI (411) mmu_psram: Read only data copied and mapped to SPIRAMᵀ[0m

V (411) esp_psram: after copy .rodata, used page is 2, start_page is 7, psram_available_size is 7929856 Bᵀ[0m

V (420) mmap: found laddr is 0x70000ᵀ[0m

V (424) esp_psram: 8bit-aligned-region: actual_mapped_len is 0x790000 bytesᵀ[0m

V (431) esp_psram: 8bit-aligned-range: 0x790000 B, starting from: 0x3c070000ᵀ[0m

ᵀ[0;32mI (438) cpu_start: Pro cpu up.ᵀ[0m

ᵀ[0;32mI (442) cpu_start: Starting app cpu, entry point is 0x40377244ᵀ[0m

ᵀ[0;32mI (0) cpu_start: App cpu up.ᵀ[0m

V CACHE_ERR: illegal error intr clr & ena mask is: 0x3f

V CACHE_ERR: core 1 access error intr clr & ena mask is: 0x1f

ᵀ[0;32mI (876) esp_psram: SPI SRAM memory test OKᵀ[0m

D (884) clk: RTC_SLOW_CLK calibration value: 3558400ᵀ[0m

V CACHE_ERR: illegal error intr clr & ena mask is: 0x3f

V CACHE_ERR: core 0 access error intr clr & ena mask is: 0x1f

ᵀ[0;32mI (890) cpu_start: Pro cpu start user codeᵀ[0m

ᵀ[0;32mI (893) cpu_start: cpu freq: 160000000 Hzᵀ[0m

ᵀ[0;32mI (898) cpu_start: Application information:ᵀ[0m

ᵀ[0;32mI (903) cpu_start: Project name: LVGLᵀ[0m

ᵀ[0;32mI (908) cpu_start: App version: 1ᵀ[0m

ᵀ[0;32mI (912) cpu_start: Compile time: Mar 6 2024 15:25:07ᵀ[0m

ᵀ[0;32mI (918) cpu_start: ELF file SHA256: 7b9f72d62b1bf1af...ᵀ[0m

ᵀ[0;32mI (924) cpu_start: ESP-IDF: 5.1.2ᵀ[0m

ᵀ[0;32mI (929) cpu_start: Min chip rev: v0.0ᵀ[0m

ᵀ[0;32mI (933) cpu_start: Max chip rev: v0.99 ᵀ[0m

ᵀ[0;32mI (938) cpu_start: Chip rev: v0.2ᵀ[0m

V (943) memory_layout: reserved range is 0x3c066184 - 0x3c0661b4ᵀ[0m

D (949) memory_layout: Checking 7 reserved memory ranges:ᵀ[0m

D (955) memory_layout: Reserved memory range 0x3c000000 - 0x3e000000ᵀ[0m

D (961) memory_layout: Reserved memory range 0x3fc84000 - 0x3fc96100ᵀ[0m

D (967) memory_layout: Reserved memory range 0x3fc96100 - 0x3fca22f0ᵀ[0m

D (974) memory_layout: Reserved memory range 0x3fceee34 - 0x3fcf0000ᵀ[0m

D (980) memory_layout: Reserved memory range 0x40374000 - 0x40386100ᵀ[0m

D (987) memory_layout: Reserved memory range 0x600fe000 - 0x600fe010ᵀ[0m

D (993) memory_layout: Reserved memory range 0x600fffe8 - 0x60100000ᵀ[0m

D (1000) memory_layout: Building list of available memory regions:ᵀ[0m

V (1006) memory_layout: Examining memory region 0x3c000000 - 0x3e000000ᵀ[0m

V (1012) memory_layout: Region 0x3c000000 - 0x3e000000 inside of reserved 0x3c000000 - 0x3e000000ᵀ[0m

V (1021) memory_layout: Examining memory region 0x40374000 - 0x40378000ᵀ[0m

V (1028) memory_layout: Region 0x40374000 - 0x40378000 inside of reserved 0x40374000 - 0x40386100ᵀ[0m

V (1037) memory_layout: Examining memory region 0x3fc88000 - 0x3fc90000ᵀ[0m

V (1044) memory_layout: Region 0x3fc88000 - 0x3fc90000 inside of reserved 0x3fc84000 - 0x3fc96100ᵀ[0m

V (1053) memory_layout: Examining memory region 0x3fc90000 - 0x3fca0000ᵀ[0m

V (1059) memory_layout: Start of region 0x3fc90000 - 0x3fca0000 overlaps reserved 0x3fc84000 - 0x3fc96100ᵀ[0m

V (1069) memory_layout: Region 0x3fc96100 - 0x3fca0000 inside of reserved 0x3fc96100 - 0x3fca22f0ᵀ[0m

V (1078) memory_layout: Examining memory region 0x3fca0000 - 0x3fcb0000ᵀ[0m

V (1085) memory_layout: Start of region 0x3fca0000 - 0x3fcb0000 overlaps reserved 0x3fc96100 - 0x3fca22f0ᵀ[0m

D (1094) memory_layout: Available memory region 0x3fca22f0 - 0x3fcb0000ᵀ[0m

V (1101) memory_layout: Examining memory region 0x3fcb0000 - 0x3fcc0000ᵀ[0m

D (1108) memory_layout: Available memory region 0x3fcb0000 - 0x3fcc0000ᵀ[0m

V (1114) memory_layout: Examining memory region 0x3fcc0000 - 0x3fcd0000ᵀ[0m

D (1121) memory_layout: Available memory region 0x3fcc0000 - 0x3fcd0000ᵀ[0m

V (1128) memory_layout: Examining memory region 0x3fcd0000 - 0x3fce0000ᵀ[0m

D (1134) memory_layout: Available memory region 0x3fcd0000 - 0x3fce0000ᵀ[0m

V (1141) memory_layout: Examining memory region 0x3fce0000 - 0x3fce9710ᵀ[0m

D (1148) memory_layout: Available memory region 0x3fce0000 - 0x3fce9710ᵀ[0m

V (1154) memory_layout: Examining memory region 0x3fce9710 - 0x3fcf0000ᵀ[0m

V (1161) memory_layout: End of region 0x3fce9710 - 0x3fcf0000 overlaps reserved 0x3fceee34 - 0x3fcf0000ᵀ[0m

D (1171) memory_layout: Available memory region 0x3fce9710 - 0x3fceee34ᵀ[0m

V (1177) memory_layout: Examining memory region 0x3fcf0000 - 0x3fcf8000ᵀ[0m

D (1184) memory_layout: Available memory region 0x3fcf0000 - 0x3fcf8000ᵀ[0m

V (1191) memory_layout: Examining memory region 0x600fe000 - 0x60100000ᵀ[0m

V (1197) memory_layout: Start of region 0x600fe000 - 0x60100000 overlaps reserved 0x600fe000 - 0x600fe010ᵀ[0m

V (1207) memory_layout: End of region 0x600fe010 - 0x60100000 overlaps reserved 0x600fffe8 - 0x60100000ᵀ[0m

D (1216) memory_layout: Available memory region 0x600fe010 - 0x600fffe8ᵀ[0m

ᵀ[0;32mI (1223) heap_init: Initializing. RAM available for dynamic allocation:ᵀ[0m

D (1230) heap_init: New heap initialised at 0x3fca22f0ᵀ[0m

ᵀ[0;32mI (1236) heap_init: At 3FCA22F0 len 00047420 (285 KiB): DRAMᵀ[0m

ᵀ[0;32mI (1242) heap_init: At 3FCE9710 len 00005724 (21 KiB): STACK/DRAMᵀ[0m

D (1249) heap_init: New heap initialised at 0x3fcf0000ᵀ[0m

ᵀ[0;32mI (1254) heap_init: At 3FCF0000 len 00008000 (32 KiB): DRAMᵀ[0m

D (1260) heap_init: New heap initialised at 0x600fe010ᵀ[0m

ᵀ[0;32mI (1265) heap_init: At 600FE010 len 00001FD8 (7 KiB): RTCRAMᵀ[0m

ᵀ[0;32mI (1272) esp_psram: Adding pool of 7744K of PSRAM memory to heap allocatorᵀ[0m

V (1279) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵀ[0m

V (1286) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0x40Eᵀ[0m

D (1294) intr_alloc: Connected src 39 to int 2 (cpu 0)ᵀ[0m

V (1299) memspi: raw_chip_id: 1740C8

ᵀ[0m

V (1303) memspi: chip_id: C84017

ᵀ[0m

V (1306) memspi: raw_chip_id: 1740C8

ᵀ[0m

V (1310) memspi: chip_id: C84017

ᵀ[0m

D (1314) spi_flash: trying chip: issiᵀ[0m

D (1317) spi_flash: trying chip: gdᵀ[0m

ᵀ[0;32mI (1321) spi_flash: detected chip: gdᵀ[0m

ᵀ[0;32mI (1325) spi_flash: flash io: dioᵀ[0m

D (1329) cpu_start: calling init function: 0x4203491cᵀ[0m

D (1335) cpu_start: calling init function: 0x420338a0ᵀ[0m

D (1340) cpu_start: calling init function: 0x42031450ᵀ[0m

D (1345) cpu_start: calling init function: 0x42035a2c on core: 0ᵀ[0m

V (1351) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵀ[0m

V (1357) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0xC02ᵀ[0m

D (1365) intr_alloc: Connected src 59 to int 3 (cpu 0)ᵀ[0m

D (1371) cpu_start: calling init function: 0x420489b8 on core: 0ᵺ[0m

ᵺ[0;32mI (1377) sleep: Configure to isolate all GPIO pins in sleep stateᵺ[0m

ᵺ[0;32mI (1384) sleep: Enable automatic switching of GPIO sleep configurationᵺ[0m

D (1391) cpu_start: calling init function: 0x42035798 on core: 0ᵺ[0m

V (1397) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵺ[0m

V (1403) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0x40Eᵺ[0m

D (1411) intr_alloc: Connected src 79 to int 9 (cpu 0)ᵺ[0m

ᵺ[0;32mI (1417) app_start: Starting scheduler on CPU0ᵺ[0m

V (1422) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵺ[0m

V (1422) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0x402ᵺ[0m

D (1422) intr_alloc: Connected src 57 to int 12 (cpu 0)ᵺ[0m

V (1422) intr_alloc: esp_intr_alloc_intrstatus (cpu 1): checking argsᵺ[0m

V (1432) intr_alloc: esp_intr_alloc_intrstatus (cpu 1): Args okay. Resulting flags 0x40Eᵺ[0m

D (1432) intr_alloc: Connected src 80 to int 2 (cpu 1)ᵺ[0m

ᵺ[0;32mI (1442) app_start: Starting scheduler on CPU1ᵺ[0m

V (1442) intr_alloc: esp_intr_alloc_intrstatus (cpu 1): checking argsᵺ[0m

V (1452) intr_alloc: esp_intr_alloc_intrstatus (cpu 1): Args okay. Resulting flags 0x402ᵺ[0m

D (1462) intr_alloc: Connected src 58 to int 3 (cpu 1)ᵺ[0m

ᵺ[0;32mI (1422) main_task: Started on CPU0ᵺ[0m

D (1472) heap_init: New heap initialised at 0x3fce9710ᵺ[0m

ᵺ[0;32mI (1472) esp_psram: Reserving pool of 32K of internal memory for DMA/internal allocationsᵺ[0m

D (1482) esp_psram: Allocating block of size 32768 bytesᵺ[0m

V (1492) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵺ[0m

V (1492) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0xEᵺ[0m

D (1502) intr_alloc: Connected src 52 to int 13 (cpu 0)ᵺ[0m

ᵺ[0;32mI (1512) main_task: Calling app_main()ᵺ[0m

ᵺ[0;32mI (1512) lvgl_helpers: Display buffer size: 19200ᵺ[0m

ᵺ[0;32mI (1522) lvgl_helpers: Initializing SPI master for displayᵺ[0m

ᵺ[0;32mI (1522) lvgl_helpers: Configuring SPI host SPI2_HOSTᵺ[0m

ᵺ[0;32mI (1532) lvgl_helpers: MISO pin: 12, MOSI pin: 13, SCLK pin: 14, IO2/WP pin: -1, IO3/HD pin: -1ᵺ[0m

ᵺ[0;32mI (1542) lvgl_helpers: Max transfer size: 57600 (bytes)ᵺ[0m

ᵺ[0;32mI (1552) lvgl_helpers: Initializing SPI bus...ᵺ[0m

D (1552) gdma: new group (0) at 0x3c070934ᵺ[0m

D (1552) gdma: new pair (0,0) at 0x3c070978ᵀ[0m

D (1562) gdma: new tx channel (0,0) at 0x3c070900ᵀ[0m

D (1562) gdma: new rx channel (0,0) at 0x3c070998ᵀ[0m

D (1572) spi: SPI2 use gpio matrix.ᵀ[0m

ᵀ[0;32mI (1572) disp_spi: Adding SPI deviceᵀ[0m

ᵀ[0;32mI (1582) disp_spi: Clock speed: 1000000Hz, mode: 0, CS pin: 15ᵀ[0m

V (1582) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking argsᵀ[0m

V (1592) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0x80Eᵀ[0m

D (1602) intr_alloc: Connected src 21 to int 17 (cpu 0)ᵀ[0m

V (1602) bus_lock: device registered on bus 1 slot 0.ᵀ[0m

D (1612) spi_hal: eff: 1000, limit: 80000k(/0), 0 dummy, -1 delayᵀ[0m

D (1612) spi_master: SPI2: New device added to CS0, effective clock: 1000kHzᵀ[0m

ᵀ[0;32mI (1822) ILI9488: ILI9488 initialization.ᵀ[0m

V bus_lock: dev 0 acquired.

V (1822) spi_master: polling transᵀ[0m

V bus_lock: SPI dev changed from -1 to 0

V (1822) spi_master: polling trans doneᵀ[0m

V (1822) bus_lock: dev 0 released.ᵀ[0m

V bus_lock: dev 0 acquired.

V (1932) spi_master: polling transᵀ[0m

V (1932) spi_master: polling trans doneᵀ[0m

V (1932) bus_lock: dev 0 released.ᵀ[0m

V bus_lock: dev 0 acquired.

V (2032) spi_master: polling transᵀ[0m

V (2032) spi_master: polling trans doneᵀ[0m

V (2032) bus_lock: dev 0 released.ᵀ[0m

V bus_lock: dev 0 acquired.

V (2032) spi_master: polling transᵀ[0m

V (2032) spi_master: polling trans doneᵀ[0m

V (2042) bus_lock: dev 0 released.ᵀ[0m

V bus_lock: dev 0 acquired.

V (2042) spi_master: polling transᵀ[0m

V (2052) spi_master: polling trans doneᵀ[0m

V (2052) bus_lock: dev 0 released.ᵀ[0m

V bus_lock: dev 0 acquired.

V (2062) spi_master: polling trans[0m

V (2062) spi_master: polling trans done[0m

V (2062) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2072) spi_master: polling trans[0m

V (2072) spi_master: polling trans done[0m

V (2082) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2082) spi_master: polling trans[0m

V (2092) spi_master: polling trans done[0m

V (2092) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2102) spi_master: polling trans[0m

V (2102) spi_master: polling trans done[0m

V (2102) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2112) spi_master: polling trans[0m

V (2112) spi_master: polling trans done[0m

V (2122) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2122) spi_master: polling trans[0m

V (2132) spi_master: polling trans done[0m

V (2132) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2142) spi_master: polling trans[0m

V (2142) spi_master: polling trans done[0m

V (2142) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2152) spi_master: polling trans[0m

V (2152) spi_master: polling trans done[0m

V (2162) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2162) spi_master: polling trans[0m

V (2172) spi_master: polling trans done[0m

V (2172) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2182) spi_master: polling trans[0m

V (2182) spi_master: polling trans done[0m

V (2182) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2192) spi_master: polling trans[0m

V (2192) spi_master: polling trans done[0m

V (2202) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2202) spi_master: polling trans[0m

V (2212) spi_master: polling trans done[0m

V (2212) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2222) spi_master: polling trans[0m

V (2222) spi_master: polling trans done[0m

V (2222) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2232) spi_master: polling trans[0m

V (2232) spi_master: polling trans done[0m

V (2242) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2242) spi_master: polling trans[0m

V (2252) spi_master: polling trans done[0m

V (2252) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2262) spi_master: polling trans[0m

V (2262) spi_master: polling trans done[0m

V (2262) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2272) spi_master: polling trans[0m

V (2272) spi_master: polling trans done[0m

V (2282) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2282) spi_master: polling trans[0m

V (2292) spi_master: polling trans done[0m

V (2292) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2302) spi_master: polling trans[0m

V (2302) spi_master: polling trans done[0m

V (2302) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2312) spi_master: polling trans[0m

V (2312) spi_master: polling trans done[0m

V (2322) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2322) spi_master: polling trans[0m

V (2332) spi_master: polling trans done[0m

V (2332) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2342) spi_master: polling trans[0m

V (2342) spi_master: polling trans done[0m

V (2342) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2352) spi_master: polling trans[0m

V (2352) spi_master: polling trans done[0m

V (2362) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2362) spi_master: polling trans[0m

V (2372) spi_master: polling trans done[0m

V (2372) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2382) spi_master: polling trans[0m

V (2382) spi_master: polling trans done[0m

V (2382) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2392) spi_master: polling trans[0m

V (2392) spi_master: polling trans done[0m

V (2402) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2402) spi_master: polling trans[0m

V (2412) spi_master: polling trans done[0m

V (2412) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2422) spi_master: polling trans[0m

V (2422) spi_master: polling trans done[0m

V (2422) bus_lock: dev 0 released.[0m

[0;32mI (2532) ILI9488: Display orientation: LANDSCAPE[0m

[0;32mI (2532) ILI9488: 0x36 command value: 0x28[0m

V bus_lock: dev 0 acquired.

V (2532) spi_master: polling trans[0m

V (2532) spi_master: polling trans done[0m

V (2532) bus_lock: dev 0 released.[0m

V bus_lock: dev 0 acquired.

V (2542) spi_master: polling trans[0m

V (2542) spi_master: polling trans done[0m

V (2552) bus_lock: dev 0 released.[0m

[0;32mI (2552) GUI_mng: Initialize LVGL library[0m

[0;32mI (2562) GUI_mng: Allocate separate LVGL draw buffers from PSRAM[0m

[0;32mI (2562) GUI_mng: Register display driver to LVGL[0m

[0;32mI (2572) TOUCH_GT911: Inilizating I2C[0m

V (2572) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): checking args[0m

V (2582) intr_alloc: esp_intr_alloc_intrstatus (cpu 0): Args okay. Resulting flags 0xE[0m

D (2592) intr_alloc: Connected src 42 to int 18 (cpu 0)[0m

[0;32mI (2592) TOUCH_GT911: GT911 is Initilazing[0m

D (2602) lcd_panel.io.i2c: new i2c lcd panel io @0x3fcc288c[0m

[0;32mI (2602) gpio: GPIO[16]| InputEn: 1| OutputEn: 0| OpenDrain: 0| Pullup: 0| Pulldown: 0| Intr:2 [0m

[0;32mI (2612) gpio: GPIO[8]| InputEn: 0| OutputEn: 1| OpenDrain: 0| Pullup: 0| Pulldown: 0| Intr:0 [0m

[0;32mI (2642) GT911: TouchPad_ID:0x39,0x31,0x31[0m

[0;32mI (2642) GT911: TouchPad_Config_Version:0[0m

[0;32mI (2642) GUI_mng: Configure Touch to LVGL Register[0m

ESPS3 REBOOT error.

ESP-ROM:esp32s3-20210327

Build:Mar 27 2021

rst:0x7 (TG0WDT_SYS_RST),boot:0x2a (SPI_FAST_FLASH_BOOT)

Saved PC:0x40041a76

SPIWP:0xee